REMARKS

Claim Rejections Under 35 U.S.C. §§ 102(b) and 103(a)

Claims 1-28 are pending. Claims 1-3, 19, 20, 24, and 25 stand rejected under 35 U.S.C. § 102(b)[1] as being anticipated by United States Patent Application Publication No. 2003/0233394 ("Rudd"), and claims 4-14, 21-23 and 26-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rudd.

Applicants amend claims 13, 23, and 28 by rewriting them in independent form to incorporate the limitation of their base claims and any intervening claims. Claims 2, 3, 12, and 14 are amended so that they ultimately depend from claim 13; claim 22 is amended so that it depends from claim 23; and claim 27 is amended so that it depends from claim 28.

Amended independent claims 13, 23 and 28 are patentable over Rudd because they each recite a feature not disclosed or suggested in Rudd: setting a priority thread value equal to the internal thread value when the maxtime value corresponding to the internal thread value is not equal to zero. Rudd does not disclose checking whether the threshold or limit of a thread's forward progress counter, which is equivalent to the maxtime register value, equals zero *prior to* designating the thread as the currently executing (i.e., priority) thread. *See* Rudd at ¶ 0035. In Rudd, when the currently executing thread is switched out, another thread becomes the currently executing (priority) thread without first checking whether its limit or threshold equals zero. Claims 13, 23, and 28 recite a limitation that would not permit such a thread to become the priority thread.

Claims 15-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rudd in view of United States Patent No. 6,567,839 ("Borkenhagen"). Claim 15 recites an execution thread comprising, among other things, "a thread block checker configured to provide a plurality of block values, wherein each active thread has a corresponding block value." Claims 16-18 ultimately depend from claim 15.

[1] The rejection under 35 U.S.C. § 102(b) is improper, as Rudd was published on December 18, 2003, less than one year before the instant application was filed. The rejection should have been issued pursuant to 35 U.S.C. § 102(e), and Applicants respectfully request that the Examiner revise the rejection accordingly.

Applicants amend claim 15 by rewriting it in independent form to include all of the limitations of base claim 1. Applicants also amend claims 16-18 to reflect that they ultimately depend from claim 15.

The Examiner argues that the thread block checker of claim 15 is disclosed in Borkenhagen as the thread switch control register 410 of Figure 4A. Applicants respectfully traverse because the thread switch control register does not contain the block value corresponding to each active thread, as required by amended claim 15. Rather, the thread switch control register stores a plurality of block values for each thread such that if one of those block values is determined to correspond to a given thread, the thread would be considered blocked. *See* Borkenhagen, col. 12, ll. 65-66. The thread switch control register does not actually provide the corresponding block value as required by amended claim 15. For at least this reason, the thread block checker of amended claims 15-18 is neither disclosed nor suggested in Borkenhagen.

Claims 1-14 and 19-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 5,528,513 ("Vaitzblit") in view of United States Patent Publication No. 2003/0154235 ("Sager"), and claims 15-18 stand rejected over Vaitzblit in view of Sager and further in view of Borkenhagen.

Applicants amend independent claims 13, 15, 23 and 28 to include a limitation reciting the existence of a "plurality of active threads in the multithreaded microprocessor."

The Examiner argues that Vaitzblit teaches a thread selection unit for a multithreaded processor having a plurality of active threads, but Vaitzblit neither discloses nor suggests a multithreaded processor with a plurality of active threads. Vaitzblit teaches a CPU 50 and a scheduler 53, not located in the CPU, where the scheduler maintains a GP ready queue 108 of threads to be executed in the CPU according to an algorithm implemented by the scheduler. Nothing in Vaitzblit discloses or suggests that the CPU 50 is multithreaded or, even if it were multithreaded, that the plurality of threads 102, 104, 106 in the GP ready queue are active in the multithreaded processor. For at least this reason, a multithreaded microprocessor having a plurality of active threads is neither disclosed nor suggested in Vaitzblit.

Claim Rejections Under 35 U.S.C. § 112

Claim 8 was rejected under 35 U.S.C. § 112, first paragraph, for failing to comply with the enablement requirement. As claim 8 has been cancelled, this rejection is moot.

Claims 8, 10, 12, 13, 14 and 16 were rejected under 35 U.S.C. § 112, second paragraph. Claims 12, 13, 14 and 16 have been amended to remedy the deficiencies cited by the Examiner. As claims 8 and 10 have been cancelled, this rejection is moot as to those claims.

Claim Objection

The Examiner objected to the claims because there are two claims numbered "13," and the claims which followed are thus misnumbered by 1. Applicants have amended the misnumbered claims to correct this deficiency.

Specification Objections

The Examiner identified two errors in the specification. Applicants have amended the specification to correct these errors as suggested by the Examiner.

Drawing Objection

The Examiner objected to the drawings because they illustrate that the maxtime registers and the threads are both identified by an integer value N with possible values 0 through N-1. According to the Examiner, one skilled in the art would recognize that threads are not identified by integer values, but rather by pointers indicating either the referencing data stream or the context register location. Thus, the Examiner argues that the specification, and thus the drawings, should indicate the use of two separate indices for the maxtime registers and the actual threads.

Applicants respectfully traverse this objection. One with skill in the art would appreciate that the integers 0 to N-1 used to refer to threads are pointers to the active threads, and that maxtime[N] is an array of pointers to the registers on the processor used to store the maxtime values corresponding to the active threads, such that maxtime[n] corresponds to thread n. One with skill in the art would be able to implement this scheme without amendments to the drawings that

distinguish between the maxtime register indices and thread values. If anything, such an amendment would serve only to unnecessarily complicate the disclosure.

Applicants have responded to all of the rejections and objections recited in the Office Action. Reconsideration and a Notice of Allowance for claims 2-3, 12-18, 20, 22-23, 25, and 27-28 is therefore respectfully requested.

In view of the above, claims 2-3, 12-18, 20, 22-23, 25, and 27-28 are believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejections of and objections to the claims and to pass this application to issue.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

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Respectfully submitted,

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